IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **FUKASAWA, Shinji**

Serial No.: **09/855,590**

Filed: **May 15, 2001**

Group Art Unit: **2814**

Examiner: **Tuan N. QUACH**

P.T.O. Confirmation No.: **1417**

For: **SEMICONDUCTOR DEVICE HAVING A MULTIPLE LAYER WIRING STRUCTURE, WIRING METHOD, WIRING DEVICE, AND RECORDING MEDIUM**

PRELIMINARY AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

February 10, 2003

Sir:

Prior to examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Amend claims 1-2 and 6 as follows:

1. (Twice Amended) A semiconductor device having a multiple layer wiring structure that is provided with two or more metal layers and having a stack VIA portion for connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, comprising:

two or more partitioned intermediate metal layers that are partitioned inside the connection area; and

an intermediate metal layer wiring area that is sandwiched by the partitioned intermediate

Match and Return